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A NOVEL MULTILEVEL INVERTER TOPOLOGY FOR SYMMETRIC AND ASYMMETRIC SOURCE CONFIGURATION WITH REDUCED DEVICE COUNT

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Abstract

Multilevel inverters (MLIs) are very popular in renewable energy applications due to reduced voltage stress and less total harmonics distortion. However, in conventional two-level inverters, the number of devices increases with the increase in the number of output voltage levels, and the circuit becomes bulky and expensive. An MLI topology with the reduced number of power devices especially for the higher output levels is presented in this paper. Forty-nine levels can be generated in the output voltage waveform from this circuit by using only 12 power switches. The performance of the proposed topology is evaluated through MATLAB/Simulink in detailed simulation and power loss analysis. Theoretical analysis and simulation are presented to demonstrate the feasibility and effectiveness of the proposed MLI topology. A comparative analysis shows that the proposed MLI topology is superior to other selected existing topologies on many parameters. Finally, the simulation results the proposed MLI topology are experimentally validated using the experimental results.

Key Words

Asymmetric, cascaded MLI, multilevel Inverter (MLI), reduced device count (RDC), symmetric, total harmonic distortion (THD)

1. Introduction

Remarkable growth in renewable energy has made inverter as new frontier in DC-to-AC conversion system. Researchers are striving for a cost-effective and efficient high-power voltage source multilevel inverter (MLI). Generation of staircase waveform is realized through multiple DC sources and power switches. The MLI offers benefits of (i) low voltage stress on switches as compared with operating voltages, and (ii) better harmonic profile in comparison to conventional bi-level inverters [1]. Obligatory need of high-quality power supplies brings MLI into recent limelight.

As modern loads are sensitive to electrical fluctuations, they demand high-quality power supply. Conventional topologies such as neutral point clamped (NPC), flying capacitor (FC), and cascaded H-Bridge (CHB) converters need more number of switches for increased number of levels, making the system complex and unreliable for increased driver circuit and protection circuit requirements. Among these topologies, the CHB is most popular because of its modularity and easy extension for higher voltage requirement [2], [3].

In order to increase the voltage levels in the output, three possible circuit variations may lead to reduced number of switches and switching losses: (i) switch connections, (ii) use of asymmetric sources, and (iii) by amalgamating both methods [4]. To overcome the demerits of conventional topologies, many topologies with cross-connected switches for reduced device count (RDC) are proposed for symmetric and asymmetric configurations. However, topologies [5], [6] are not suitable for asymmetric sources as the entire additive and subtractive combination is not possible. Unlike symmetric topologies, asymmetric topologies have less device count for a defined number of voltage levels [6]. Recent topologies proposed for symmetric configuration [7], [8] are not suitable for charge balance because for symmetric configuration, it is imperative to have equal load sharing.

In [9], [10], asymmetrical source configuration topologies with different RDC have been presented. Multilevel operation at high voltage requires some of the switches to be operated at a higher voltage [11], [12]. The multilevel asymmetric topologies can produce a higher number of voltage levels in comparison to the symmetric topologies [13], [14].

This paper is organized as follows. Section 2 presents the description of basic cell structure for the proposed topology with different possible source configuration. The working principle of the topology is described in Section 3 with the help of a typical seven-level single-phase inverter. In Section 4, a generalized structure for proposed MLI is

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discussed, and the simulation results are presented. A comparison of the proposed topology with other classical recently proposed topologies is presented in Section 5. Experimental results from a laboratory prototype are presented in Section 6 for the entire configuration. Finally, conclusion followed by future work is summarized in Section 7.

2. Proposed System Description

The basic cell of the proposed MLI generates seven levels in output using two voltage sources and six switches with anti-parallel diodes as shown in Fig. 1. The basic cell uses six switches, which is the minimum in comparison to conventional MLI [2], for the same number of levels in the output. The controlled switches in the cells Q1, Q2, Q1', Q2' are arranged in conventional H-bridge configuration, while switches S1 and S2 are added to select appropriate voltage source to increase the output levels. The two basic configurations are based on the magnitude of DC sources VDC1 and VDC2. The typical seven-level output waveform is shown in Fig. 2.

2.1 Unary Configuration

The unary/symmetric source configuration consists of equal magnitude DC sources as follows:

$$V_{DC1} = V_{DC2} = V_{DC3} = \ldots\ldots\ldots = V_{DCN} = V_{DC} \quad (1)$$

A single basic cell operated in this configuration can generate five levels, which include two positive levels ($+2V_{DC}$ and $+V_{DC}$), two negative levels ($-2V_{DC}$ and $-V_{DC}$), and

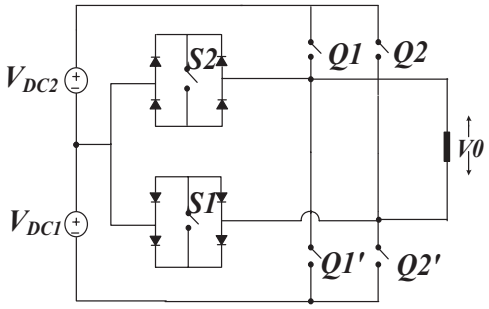


Figure 1. Basic cell for proposed topology.

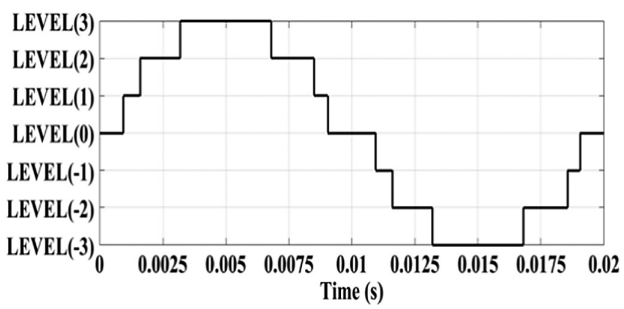


Figure 2. Typical seven-level output waveform.

Table 1
Switching States for Unary Configuration

Levels	Switch states where: ON = 1, OFF = 0						Output voltage
	S1	S2	Q1	Q2	Q1'	Q2'	
1	0	0	1	0	0	1	$+2V_{DC}$
2	0	1	0	0	0	1	$+V_{DC}$
3	0	0	0	0	1	1	0
4	1	0	0	0	1	0	$-V_{DC}$
5	0	0	0	1	1	0	$-2V_{DC}$

one level corresponding to zero magnitude. Table 1 illustrates switching states required for the generation of output voltage levels.

2.2 Asymmetric Configuration

The asymmetric configuration uses DC sources of different magnitudes. To illustrate this, the asymmetric configuration with a source ratio of 0.5 is considered.

$$\frac{V_{DC1}}{V_{DC2}} = \frac{V_{DC3}}{V_{DC4}} = \ldots\ldots\ldots = \frac{V_{DCN-1}}{V_{DCN}} \quad (2)$$

Such configuration results in $(2(N+1)-1)$ levels, where N is the number of sources in the configuration. For $N = 2$, the output has three positive levels, three negative levels, and one level corresponding to zero voltage. Table 2 illustrates the switching states required for the generation of seven voltage levels at the output.

3. Operating Principle

The seven-level output in asymmetric mode operation is shown in Fig. 2. To synthesize each output level, the proposed topology operates in one distinct mode. Out of

Table 2
Switching States for Asymmetric Configuration

Levels	Switch states where: ON = 1, OFF = 0						Output voltage
	S1	S2	Q1	Q2	Q1'	Q2'	
1	0	1	0	0	0	1	$+V_{DC1}$
2	1	0	1	0	0	0	$+V_{DC2}$
3	0	0	1	0	0	1	$V_{DC1} + V_{DC2}$
4	0	0	0	0	1	1	0
5	1	0	0	0	1	0	$-V_{DC1}$
6	0	1	1	0	0	0	$-V_{DC2}$
7	0	0	0	1	1	0	$-(V_{DC1} + V_{DC2})$

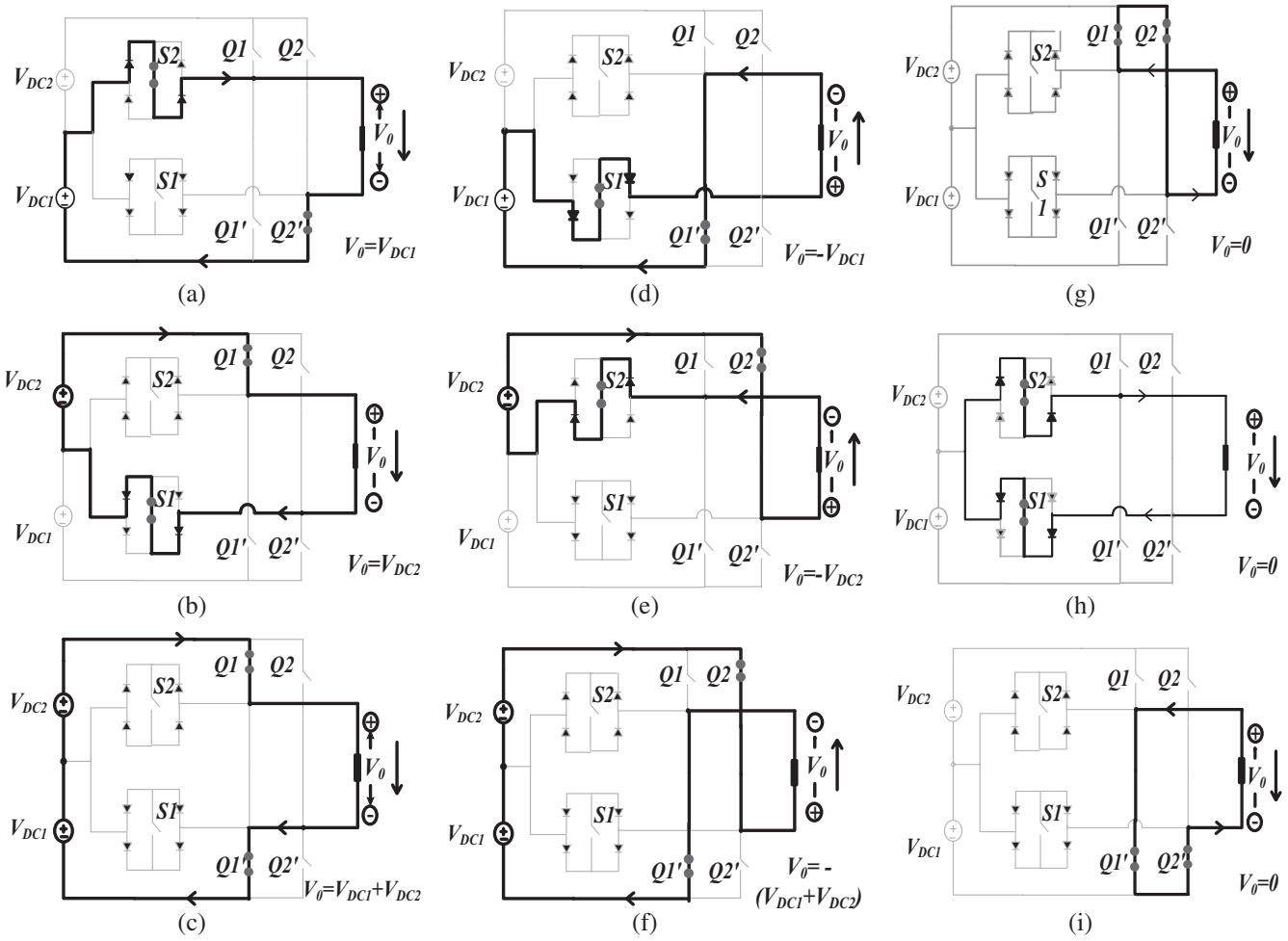


Figure 3. Different switching levels (a) 1; (b) 2; (c) 3; (d) −1; (e) −2; (f) −3; (g) 0 with circuit variation 1; (h) 0 with circuit variation 2; and (i) 0 with circuit variation 3.

the seven possible modes, the "Level-0" mode may have three circuit variations as discussed in Section 3.7.

3.1 Mode Level (3)

In mode level (1), two switches S2 and Q2' are switched ON, whereas other switches remain OFF as shown in Fig. 3(a). The output voltage is VDC1, as it is directly connected across the load. The active current path is shown with dark bold lines, and thin grey lines show the inactive path.

3.2 Mode Level (2)

The switching operations in mode level (2) generate output voltage V_{DC2}. In this mode, the switches Q1 and S1 are made ON, connecting the load directly across the source V_{DC2}, as shown in Fig. 3(b).

3.3 Mode Level (3)

In this mode, the switches Q1 and Q1' are made ON, connecting sources V_{DC1} and V_{DC2}, with additive polarity across the load. The output voltage is thus $V_{DC1} + V_{DC2}$ as shown in Fig. 3(c).

3.4 Mode Level (−1)

The output voltage in mode level (−1) is $(-V_{DC1})$. Switching the devices S1, Q1' ON simultaneously, the source V_{DC1} with reverse polarity is connected across the load, as shown in Fig. 3(d).

3.5 Mode Level (−2)

The switching operation in mode level (−2) generates output voltage (−VDC2). In this mode, switches S2, Q2 are ON, connecting the source (VDC2) with reversed polarity across the load, as shown in Fig. 3(e).

3.6 Mode Level (−3)

The switching operation in mode level (−3) made the switches Q2 & Q1' ON. As switching operation inverses the current flow through the load, the output voltage is actually $(-(V_{DC1} + V_{DC2}))$, as shown in Fig. 3(f).

3.7 Mode Level (Zero)

The switching operation in mode level (0) generates output voltage "Zero". There are three possible circuit variations

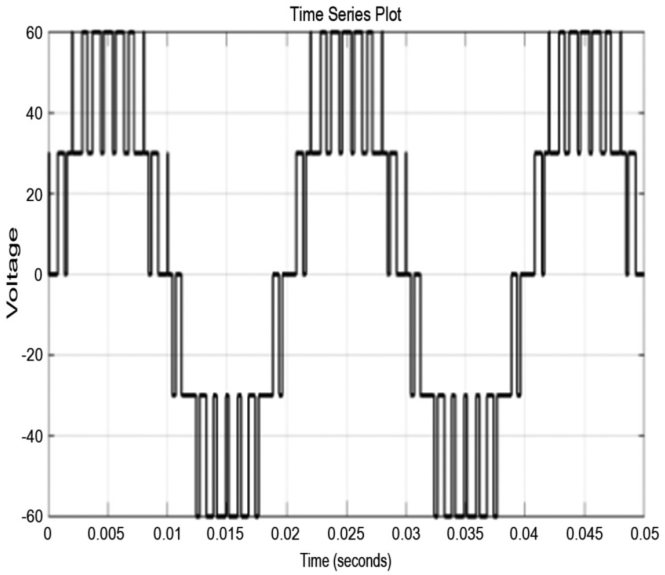


Figure 4. Simulation output for symmetrical source configuration.

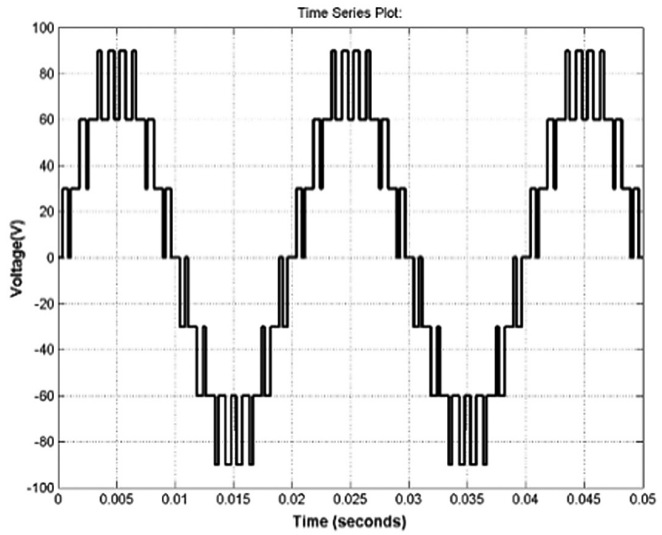


Figure 5. Simulation output for asymmetrical source configuration.

in this mode. The mode in Fig. 3(g) made two switches Q1 and Q2 ON, giving zero output voltage. The other two variations that give zero voltage are shown in Fig. 3(h) and (i).

Simulation result of the proposed topology operated in unary configuration is shown in Fig. 4. The output is symmetrical with five voltage levels. Fig. 5 exhibits seven levels in output voltage, when the same topology is operated in asymmetric configuration.

4. Generalized Analysis of Proposed Multilevel Inverter

To increase the voltage levels in the output, two or more basic cells of Fig. 1 are cascaded. The cascaded operation is performed by connecting a positive terminal of one basic cell to a negative terminal of the next cell.

4.1 Unary Mode Operation

In Unary mode, DC sources of identical magnitude are connected to all basic cells. For any given qth cell

$$V_{DCq} = V_{DC}[\text{where } q = 1, 2, \ldots .n] \tag{3}$$

Each basic cell has two equal sources, if $v^q_{\max}$ is the maximum voltage produced by qth cell, then

$$v^q_{\max} = 2V_{DC} \tag{4}$$

Let n such basic cells be connected in series, the total maximum output voltage $v_{\max}$:

$$v_{\max} = n.v^q_{\max} = 2.n..V_{DC} \tag{5}$$

Thus, the inverter output will swing between maximum voltage limits of $+v_{\max}$ to $-v_{\max}$ With n series cells, the control scheme synthesizes the inverter's output in N_L number of levels and N_s total number of source as follows:

$$N_L = 4n + 1, \quad \text{and} \quad N_s = 2.n \tag{6}$$

As each basic cell has six switches, therefore total number of switches required:

$$N_{switches} = 6.n \tag{7}$$

4.2 Asymmetric Mode Operation

In asymmetric mode, the DC sources of a proposed basic cell have unequal magnitude. Three different variations and corresponding simulation results for load $R = 50\ \Omega$ and $L = 10$ mH are discussed in this section.

4.2.1 Scheme A

In scheme A, each individual cell of cascaded operation of basic cell is identical, but voltage sources within the cell are asymmetric (unequal magnitude).

Referring to cascaded operation of basic cell, the equation for qth cell is given as follows:

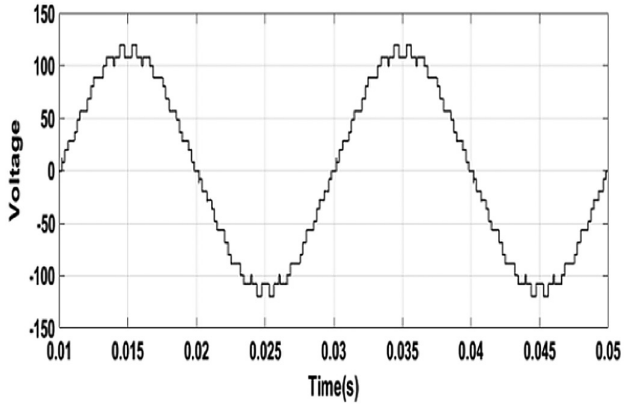
$$V_{DC2q} = V_{DC} \tag{8}$$

$$V_{DC2(q-1)} = 5^{q-1}V_{DC}[\text{where, } q = 1, 2, \ldots .n] \tag{9}$$

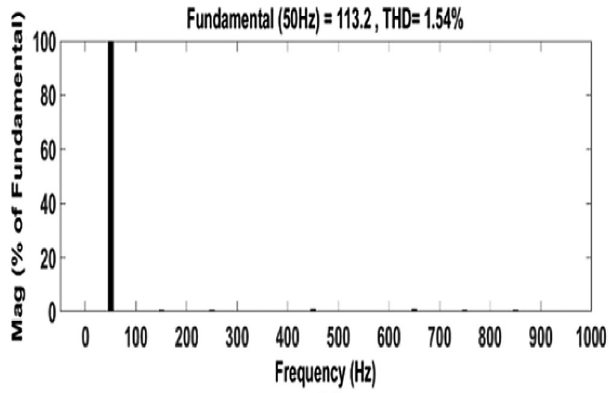
The number of sources and switches required in scheme A is the same as in unary mode *i.e.* $N_S = 2.n$ and $N_{Switches} = 6.n$, but the synthesized output voltage has multiple levels. The number of levels is given by $N_L = 5^n$. The maximum swing in inverter's output voltage $v_{\max}$ is

$$v_{\max} = \frac{5^n - 1}{2}V_{DC} \tag{10}$$

To validate the underlying principle, the proposed scheme is simulated in MATLAB/Simulink for two basic cells having source values $V_{DC1} = V_{DC2} = V_{DC} = 10$ V for $q = 1$, and $V_{DC3} = V_{DC4} = 5$. $V_{DC} = 50$ V for $q = 2$ as per (8) and (9). The output voltage shown in Fig. 6(a) has



(a)



(b)

Figure 6. (a) Asymmetric MLI: scheme A simulated output with 25 levels and (b) FFT analysis for proposed scheme A.

$N_L = 25$ levels, with maximum swing of $V_{max} = 120$ volts, as expected from (10). The FFT analysis of Fig. 6(b) has total harmonic distortion (THD) of 1.54%.

4.2.2 Scheme B

A conventional way of realizing asymmetric source configuration is defined by (2). This is alternatively termed as binary configuration. Considering the voltage ratio for binary configuration, the voltage equation for mth block can be written as follows:

$$V_{DCm} = 2^{m-1}V_{DC}[\text{where } m = 1, 2, ...2n] \quad (11)$$

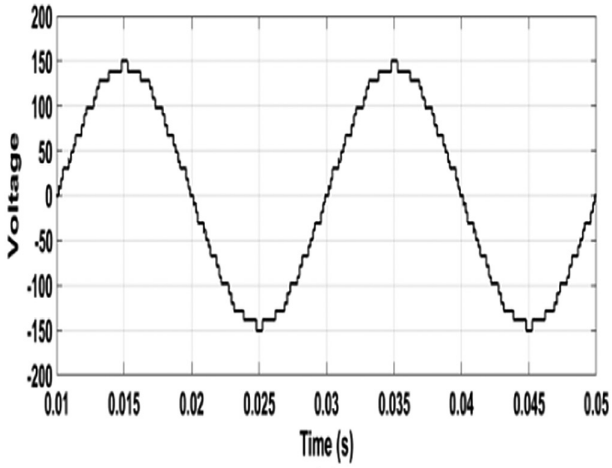
Moreover, the maximum voltage swing in inverter's output voltage:

$$v_{\max} = \pm(4^n - 1)V_{DC} \quad (12)$$

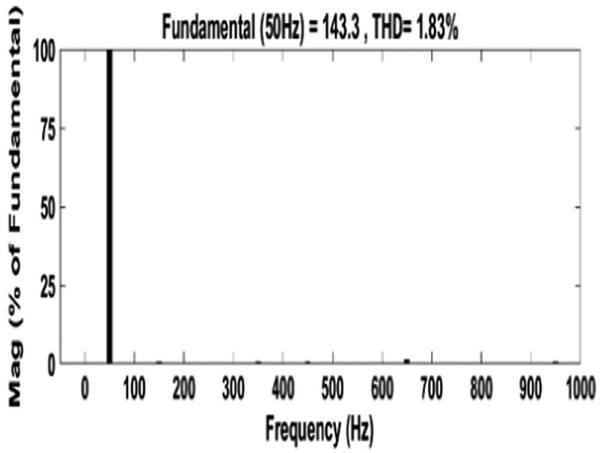
The number of sources and switches required in scheme B is the same as in scheme A, but the synthesized output voltage has number of levels given by:

$$N_L = 2^{2n+1} - 1 \quad (13)$$

To validate the basic principle, the proposed scheme B is simulated in MATLAB/Simulink environment. Considering $n = 2$, $V_{DC1} = 10$ V, $V_{DC2} = 20$ V, $V_{DC3} = 40$ V, $V_{DC4} = 80$ V, the derived equations predict a maximum value of 150 volts, with 31 levels in output voltage. The



(a)



(b)

Figure 7. (a) Asymmetric MLI: scheme B simulated output with 31 levels and (b) FFT analysis for proposed scheme B.

simulated waveforms are shown in Fig. 7(a). It complies the (12) for maximum output voltage, and (13) for the number of levels in the output. Figure 7(b) displays the harmonic content with simulated THD of 1.83% in output voltage.

4.2.3 Scheme C

To maximize the number of levels, the redundant states in inverter output must be avoided. The redundancy is eliminated by judicious choice of the voltage ratio. With n basic cells in series, the optimized value of mth DC source:

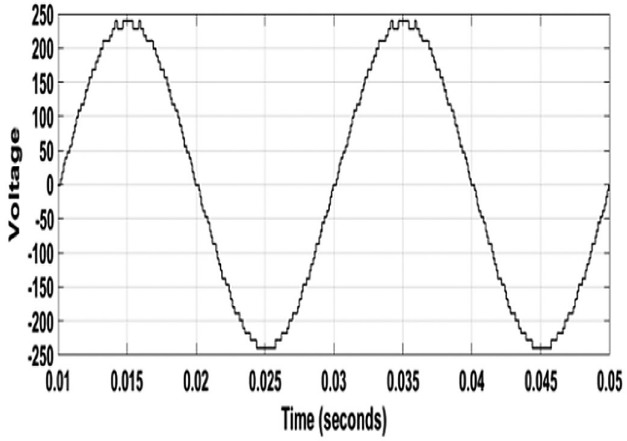
$$\begin{aligned} V_{DCm} &= 7^{\frac{m-1}{2}} \ for\ m = odd, \\ V_{DCm} &= 2 * 7^{\frac{m-2}{2}} \ for\ m = even \end{aligned} \quad (14)$$

The number of sources, switches, and levels of synthesized output voltage can be derived as follows:

$$N_s = 2.n, N_{switches} = 6.n, \ and\ N_L = 7^n \quad (15)$$

The positive and negative maximum voltage swings in the output can be given as follows:

$$v_{\max} = \frac{+(7^n - 1)}{2}V_{DC}, \ and\ v_{\max} = \frac{-(7^n - 1)}{2}V_{DC} \quad (16)$$



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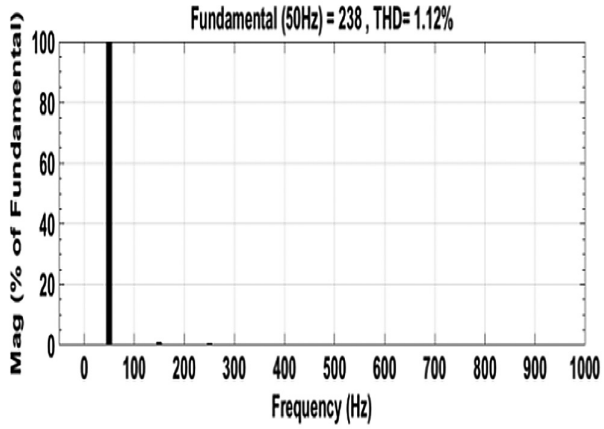

(b)

Figure 8. (a) Asymmetric MLI: scheme B simulated output with 49 levels and (b) FFT analysis for proposed scheme C.

By eliminating redundancy, the number of levels in output voltage has increased to 49 in comparison to scheme A or scheme B which have 25 and 31 levels, respectively.

The MATLAB/Simulink simulation for $n = 2$, $V_{DC1} =$ 10 V, $V_{DC2} = 20$ V, $V_{DC3} = 70$ V, $V_{DC4} = 140$ V, is shown in Fig. 8. The maximum voltage swing and number of levels in simulation result comply with (15) and (16). The proposed work significantly reduces the device count for the same number of levels in output voltage. The simulation results of Fig. 8(b) reveal THD of 1.12%, a positive improvement over scheme A and scheme B that have THD of 1.54% and 1.83%, respectively.

4.3 Power Loss and Efficiency Analysis

Conduction and switching are two types of losses, which are associated with power semiconductor devices (IGBTs (GW30NC120HD) and diodes). The conduction loss (P_C) is due to ON-state switch current maintained by ON-state voltage when power device is fully ON. Consequently, the conduction power losses of an IGBT ($P_{C,IGBT}$) and a diode ($P_{C,Diode}$) can be written as follows:

$$P_{C,IGBT} = n_{IGBT}(t) \times \left[\frac{1}{2\prod}\int_0^{2\Pi}\left[V_{ON,IGBT}I + R_{ON,IGBT}I^{\beta+1}d(\omega t)\right]\right] \quad (17)$$

$$P_{C,Diode} = n_{Diode}(t) \times \left[\frac{1}{2\prod}\int_0^{2\Pi}\left[V_{ON,Diode} + R_{ON,Diode}I^2 d(\omega t)\right]\right] \quad (18)$$

$$P_C = P_{C,IGBT} + P_{C,Diode} \quad (19)$$

Where $n_{IGBT}(t)$ and $n_{Diode}(t)$ are the ON-state voltages of the IGBT and anti-parallel diode, respectively. $R_{ON,IGBT}$ and $R_{ON,Diode}$ are the equivalent resistances of the IGBT and anti-parallel diode, respectively, while constant β associated with IGBT depends on its specification. The switching loss (P_S) is the power dissipated during switch transition from ON to OFF and vice versa. Turning-on and turning-off energy loss ($E_{on,T}, E_{off,T}$) of a power switch can be calculated as follows:

$$E_{on,T} = \int_0^{ton} v(t)i(t)dt = \int_0^{ton} \times \left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_1(t-t_{on})}{t_{on}}\right)\right]dt = \frac{1}{6}V_{SW}I_1 t_{on} \quad (20)$$

$$E_{off,T} = \int_0^{t\ off} v(t)i(t)dt = \int_0^{t\ off} \times \left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_2(t-t_{off})}{t_{off}}\right)\right]dt = \frac{1}{6}V_{SW}I_2 t_{off} \quad (21)$$

Where $E_{on,T}$ and $E_{off,T}$ represent energy losses during turn-ON (t_{on}) and turn-OFF (t_{off}) period of power switch or diodes. The switching losses (P_S) are expressed according to (22).

$$P_S = \frac{1}{T}\left(N_{on}E_{on} + N_{off}E_{off}\right) \quad (22)$$

Consequently, total loss of MLI can be written as follows:

$$P_{loss} = P_{C,IGBT} + P_{C,Diode} + P_S \quad (23)$$

In this paper, the above equations are considered to calculate the power loss of the modified MLI topologies, and efficiency (η) is obtained from (24):

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (24)$$

Where P_{out} and P_{in} are the output and input powers of the MLI [14]. Considering the input voltage and load, the evaluated efficiency of 93.31% is reached for the mentioned operating point of the proposed MLI topology.

5. Comparative Analysis

This section makes a suitable comparison between the proposed MLI with other recent MLI topologies. For asymmetric source configuration, analysed and compared with topologies presented in [9]–[14]. In Table 3 illustrates a detailed comparison of the proposed MLIs topology with recent asymmetric topologies in terms of essential parameters such as number of DC sources, capacitors, switches, diodes, drivers, and number of output voltage waveforms has been investigated.

Table 3
Tabular Comparison of Proposed Topology with Other Asymmetric Topologies

Parameters	Ref. [9]	Ref. [10]	Ref. [11]	Ref. [12]	Ref. [13]	Ref. [14]	Proposed topology
No. of DC sources	2	4	2	2	2	10	4
No. of capacitors	–	–	–	1	2	–	–
No. of switches	7	16	6	6	8	21	12
No. of main diodes	7	16	6	6	8	21	24
No. of gate drivers	7	16	6	6	8	21	12
No. of output level	5	25	5	7	49	49	49

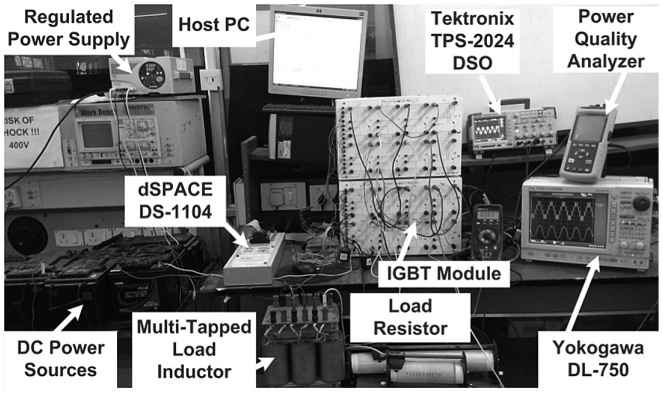

Figure 9. Experimental set-up of the proposed topology and controller.

Notably, among other recent topologies, the proposed topology requires the least number of switches for the 49 levels in the output.

6. Hardware Implementation

To verify the fundamental principle and simulation results of Section 4, a prototype of the proposed scheme is fabricated in the lab with indigenously available components.

The scheme is first simulated in MATLAB/Simulink environment and subsequently interfaced with dSPACE-1104 through Real-Time Workshop. Figure 9 is a snapshot of the complete experimental set-up.

The hardware is tested with asymmetric sources under no-load and loaded conditions. The load current and output voltage waveforms are recorded using Yokogawa power scope DL-750, and the corresponding harmonic pattern and THD are recorded using Fluke power analyser.

Fig. 10(a) shows the recorded seven-level output waveforms of voltage and current for R-L load at a switching frequency of 2,100 Hz. The voltage THD under no load is measured using power quality analyser as shown in Fig. 10(b). The measured THD is 18.5% against the theoretical value of 12.28% obtained from simulation.

Fig. 11 shows the voltage output for scheme A, as discussed in Section 4. The 25-level voltage output is obtained by selecting $V_{DC1} = V_{DC2} = 10$ V and $V_{DC3} = V_{DC4} = 50$ V. Experimental result for scheme C is shown in Fig. 12. The 49-level output is obtained by selecting $V_{DC1} = 140$ V, $V_{DC2} = 70$ V, $V_{DC3} = 20$ V, and $V_{DC4} = 10$ V.

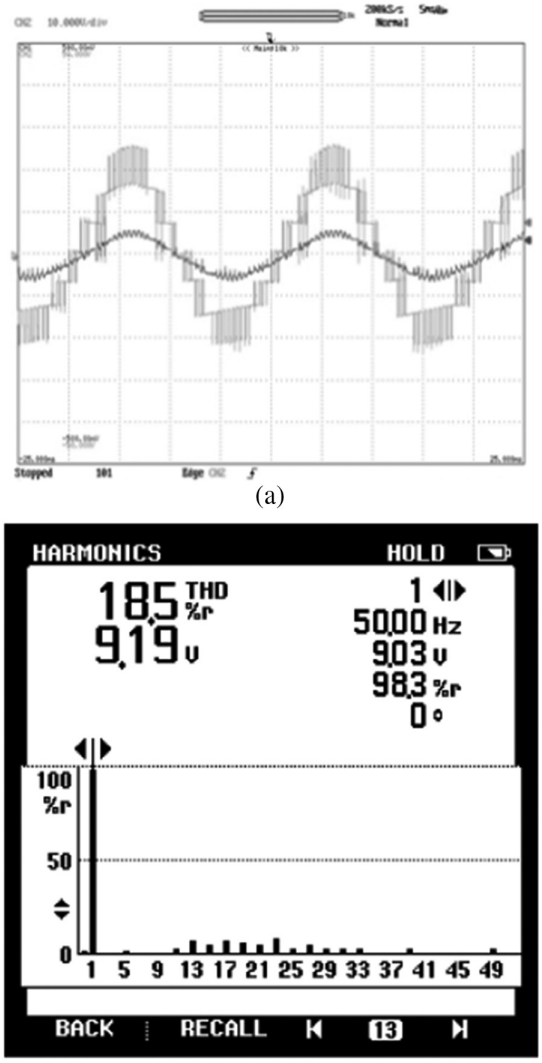

Figure 10. (a) Measured output voltage and current for RL load at 2,100 Hz switching frequency and (b) Power spectrum and THD for asymmetric voltages with RL load at 2,100 Hz switching frequency.

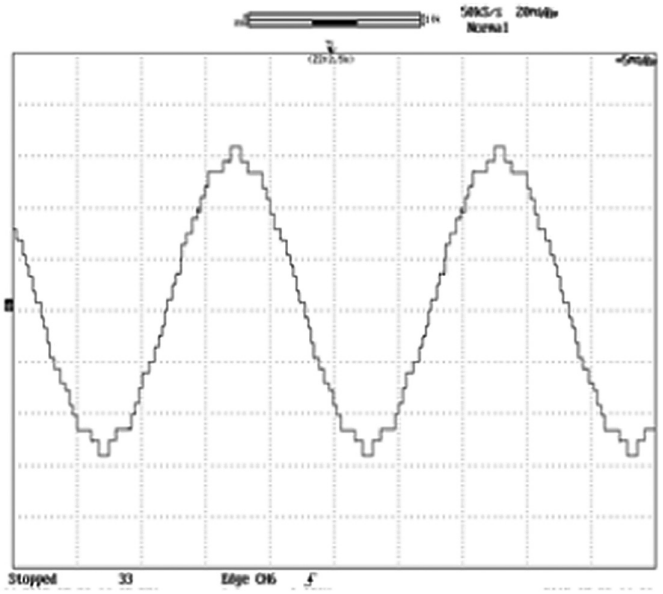

Figure 11. 25 Level voltage output of scheme A.

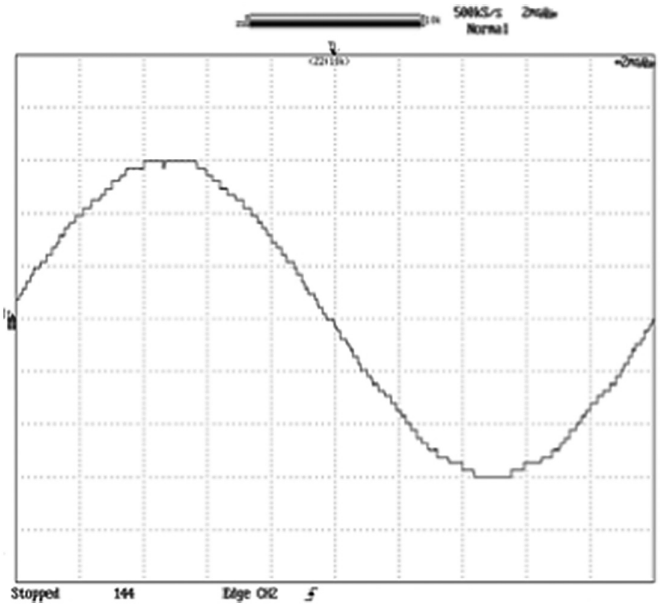

Figure 12. One cycle of 49-level output.

7. Conclusion

In this paper, a novel MLI with RDC has been proposed. A detailed description of the proposed MLI topology system and the operational principles has been presented. The working principle is explained, analysed, and verified using simulation in MATLAB/Simulink environment for both symmetric source and asymmetric source configurations. Simulation and experimental results have been obtained from a fabricated laboratory prototype of the proposed MLI to validate its effectiveness and feasibility. A detailed comparison with recent topologies has been presented to prove the superiority of switching devices, power diodes, gate driver circuits, and DC sources as well as reducing the power losses. Finally, the results agree well with the previous analyses, and the control scheme illustrates that the proposed topology is especially appropriate for modular and basic cell with high level and efficiency. The future trend involves the integration of the proposed topology in solar photovoltaic power conversion, and HVDC systems can be employed.

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